(f) initializing said status register to indicate said write operation is not suspended.

Please add the following claim:

30. A memory device, comprising;

a memory array;

a register configured to store at least one bit indicating a suspend status of a write operation;

a register configured to store at least one bit indicating a suspend status of an erase operation; and

a control circuit coupled to said memory array and said registers, said control circuit configured to update said registers and to control the outputs of status signals representing said suspend status of said write operation and said suspend status of said erase operation.

REMARKS

Reconsideration of this application as amended is respectfully requested.

Claims 1-11 and 20-25 stand rejected under 35 U.S.C. 103(a) as being unpatentable over applicants' admitted prior art or, alternatively, U.S. patent no. 5,561,628 of Terada et al. ("Terada"). Claims 12 – 19 and 26 – 29 have been withdrawn without prejudice.

The Examiner has stated that the title is not descriptive. Applicants have accordingly amended the title.

Furthermore, the Examiner has objected to the reference on page 2, line 12 to "Figure 5."

The specification has been amended to change the reference to Figure 1 instead of Figure 5.

Claims 20 – 25 have been amended to better define the invention by removing references to "steps." Moreover, new claim 30 has been added to better define the invention.

The Examiner has rejected Claims 1-11 and 20-25 under 35 U.S.C. 103(a) as being unpatentable over applicants' admitted prior art or, alternatively, Terada. The Examiner has stated in part that:

> Applicants admit that it was well known to include a status register in a memory device, including one wherein the status register includes at least one bit to indicate the suspension of an erase operation, namely ESS. The Terada reference also teaches the status register. Further, applicants discuss the relative time requirements for erase operations, programming (writing) operations and reading operations. These timings were also well known in the art. At the time of the Terada application (1994), popular microprocessor speeds were on the order of 90-100 MHZ. Recently, microprocessor speeds of 450 MHZ have been announced. The faster the processor, the greater the adverse impact of a fixed delay, such as the latency for a flash memory write. At 450 MHZ, a fixed latency impacts about 4 -1/2 times as many clock cycles as it did at 100 MHZ. Therefore, in view of the continually increasing processor speeds, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains to have provided for means to suspend the programming of a flash memory to service other requests because of the tremendous impact that latency would have on the more recent processors and the applications running on those processors. It appears that the other claimed elements to support the write operation_suspend status bit are equivalent to the support elements required for support of the prior art ESS bit, and it would therefore have been obvious to include such support elements.

(1/6/99 Office Action, p.2-3).

Applicants respectfully submit that claims 1-11 and 20-25 are not anticipated by Terada or the alleged admitted prior art. Although the admitted prior art discloses a status register with an erase suspend status indicator (ESS), that prior art teaches away from a status register with a write suspend status indicator. Applicants submit that an erase operation takes much longer time to complete than the write operation. For example, an erase operation may take a

few milliseconds ("ms"), whereas a programming operation may take 7-8 microseconds ("μs") and a reading operation may take 85 nanoseconds ("ns"). (Specification page 1, lines 22-25). A substantially larger number of reading operations can be performed in the time required to perform one erase operation than in the time required to perform one programming operation.

Applicants respectfully disagree that in view of continually increasing processor speeds, it would have been obvious at the time of the invention to suspend the programming of flash memory to service other requests. First, bus speeds have not increased as much as processor speeds. Second, although the recent processors can be at least 4 ½ times faster than the ones present at the filing date of the application, the number of read operations, for example, that may be performed in the time required to perform one programming operation (or one erase operation) has remained roughly the same. For a bus speed of 100Mhz, the bus cycle time would be 10 ns, which is substantially shorter than the read operation time of 85 ns. Thus, it is submitted that claims 1-11 and 20-25 are not obvious under 35 U.S.C. §103.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections have been overcome.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

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